REMARKS

The application has been amended and is believed to be in condition for allowance.

The Official Action objected to the drawings for being of poor quality and for Figure 4 including the identifier "s20" not discussed in the specification.

Responsively, high-quality formal drawings have been attached with Figure 4 being amended to change identifier "s20" to "p20". Withdrawal of the drawing objection is solicited.

The Official Action objected to the abstract for including reference numerals. Responsively, the abstract has been amended.

Claims 1 and 10 stand rejected as obvious over HOSHIMI et al. 4,446,490 in view of HOSHIMI et al. 4,404,602.

Claims 2-8 and 11-17 stand rejected as obvious over these two references and further in view of KOJIMA 4,459,696.

Claim 9 stands rejected as obvious over the HOSHIMI references in further view of CAMICIOTTOLI 3,760,127.

Applicant respectfully disagrees. As an overall observation, the HOSHIMI references relate to PCM signal processing circuits and do not appear to relate to intercommunicating apparatus for duplex systems. The independent claims have been amended so as to clarify the structure and nature of the invention being recited. In view of these

amendments, applicant believes it is clear that the obviousness rejection is not viable.

Although the applied references seem to have some of the functions recited in the original claims, they are not seen as having the structure recited in the amended claims.

More specifically, the HOSHIMI references cannot be found to have an output driver having its output side connected to an input side of an input driver, the output driver and input driver having the features recited. That is, an output driver having an input side connected to a first processor and receiving intercommunicating signals from that first processor, and further having an output side transmitting the intercommunicating signals in the form of a serial signal having a redundancy data structure.

Likewise, applicant does not find the recited input driver having an input side connected to the output side of the output driver, the input side receiving the serial signal having the redundancy data structure, the input driver having a further output side connected to a second processor unit.

Applicant does not see such an input driver receiving the serial signal transmitted from the output driver and reproducing from the serial signal parallel intercommunicating signals for being supplied (from the output side of the input driver) as reproduced intercommunicating signals to that second processor unit.

In view of these differences between the applied references as combined and the recitations of claim 1, reconsideration and allowance of claim 1 is respectfully requested. Claim 10 is a corresponding method claim which is believed to be allowable for the same reasons.

New dependent claim 18 recites specifically that the intercommunicating signals are those disclosed by the present application, i.e., the ACTN, SYCN, and RUNN signals. Such signals are not seen in these two HOSHIMI references.

Applicant has also added a new independent claim believed to patentably recite the present invention.

The structure recited in new independent claim 19 includes the above-discussed output driver and input driver, the input driver having a serial input serially connected to a serial output of the output driver.

The output driver is recited as comprising a parity generating circuit accepting parallel intercommunicating signals from the first processor unit and outputting the accepted signals together with a parity signal, the parity signal based on the intercommunicating signals that were accepted. Such parity generating circuit is not seen to be obvious in view of these references.

The output driver is recited as further comprising a timing generator and a parallel to serial multiplexer. The multiplexer is recited as outputting, at the serial output of the

output driver, a serial signal comprising the intercommunicating signals and the parity signal. The HOSHIMI references do not disclose such a multiplexer. Converter 6 of HOSHIMI '490 was offered as such a parallel to serial converter. However, note that the parity signal is not an input or an included output of that converter. Rather, the CRCC is added by element 7.

Likewise, see that the demulitplexer accepts the serial signal including the parity signal and provides parallel outputs including the parity signal as one of the parallel outputs..

This claim specifically recites the state holding circuit including a clear-signal line connected from the parity checker, this signal line acting to clear held content upon air detection. Such an input driver circuit is not seen from any of the applied references, taken individually or fair combination thereof.

In view of the recited combination being non-obvious over the applied art, reconsideration and allowance of claim 19 is solicited.

See that claim 20 corresponds to claim 18 and is also believed patentable.

In view of the differences noted in the independent claims and the applied references, applicant does not believe it is necessary to specifically address each of the original dependent claims. However, this is not an acknowledgement that these features are taught or obvious. The dependent claims are

believed to be allowable at least for depending from an allowable independent claim. Further, when the independent claims are properly construed, these features are believed non-obvious.

Applicant believes that the present application is in condition for allowance and an early indication of the same is respectfully requested.

The Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 25-0120 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17.

Respectfully submitted,

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APPENDIX:

The Appendix includes the following items:

- an amended Abstract of the Disclosure

- Replacement Sheets for Figures 1-5 of the drawings